

FIG. 1

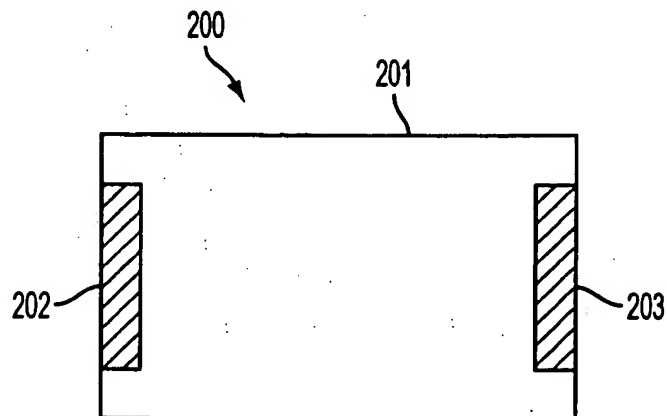


FIG. 2

Inventor: Christian IOVIN et al.
 Title of Invention: Debugging Power
 Management
 Attorney Docket No.: 42339-198723
 VENABLE

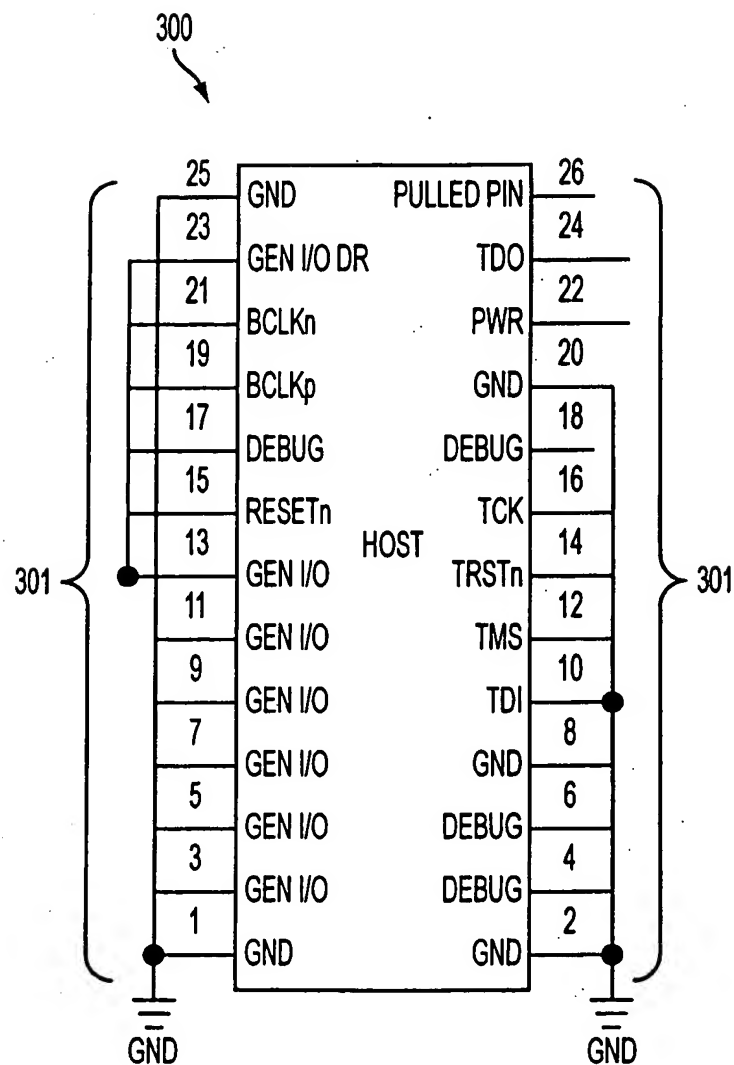


FIG. 3

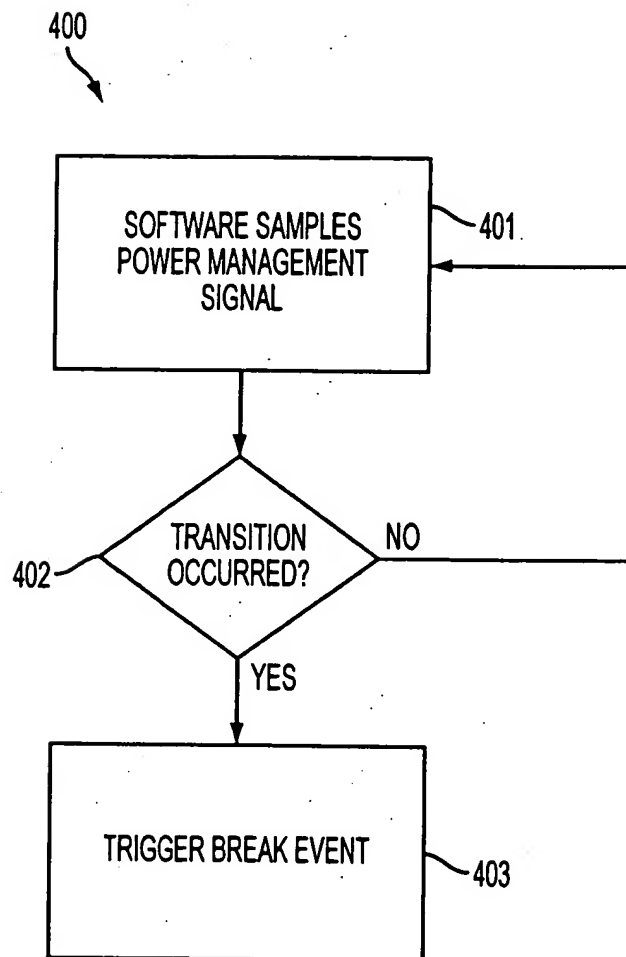


FIG. 4

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 Title of Invention: Debugging Power
 Management
 Attorney Docket No.: 42339-198723
 VENABLE

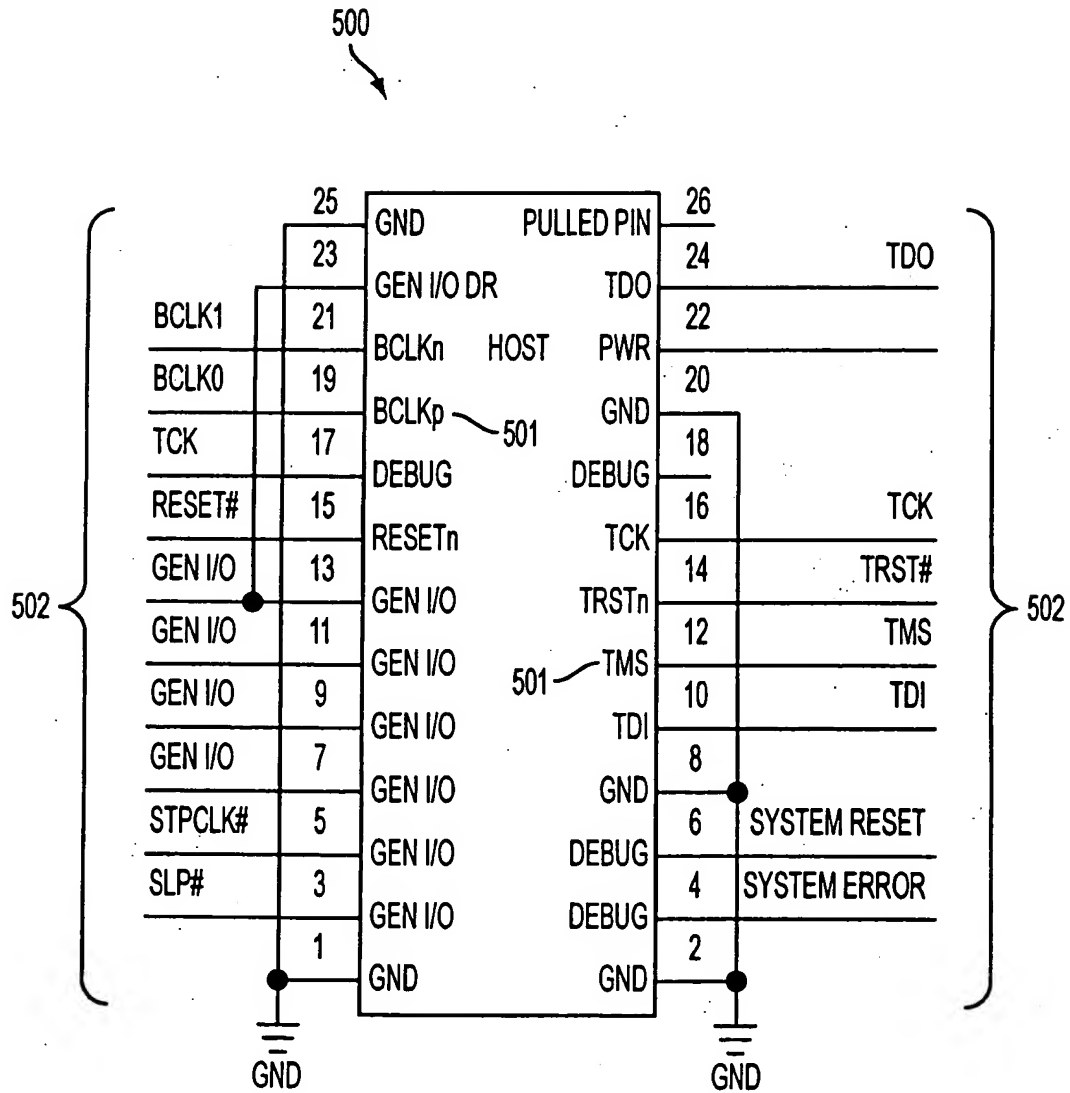


FIG. 5

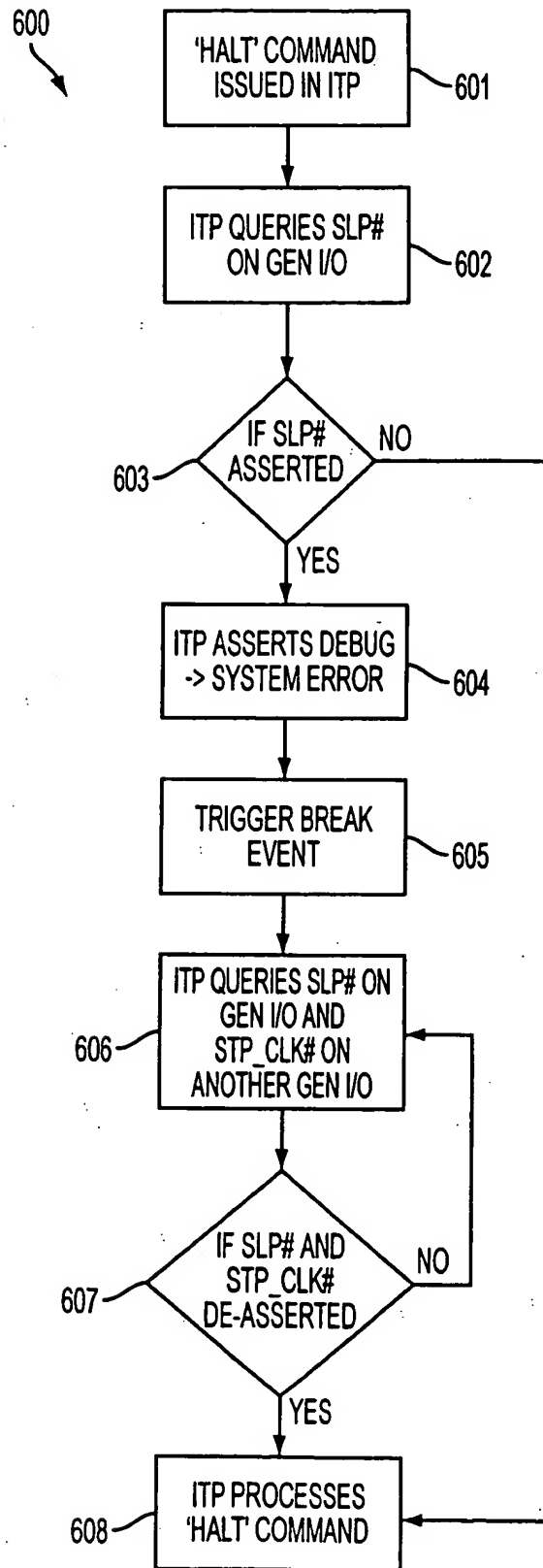


FIG. 6

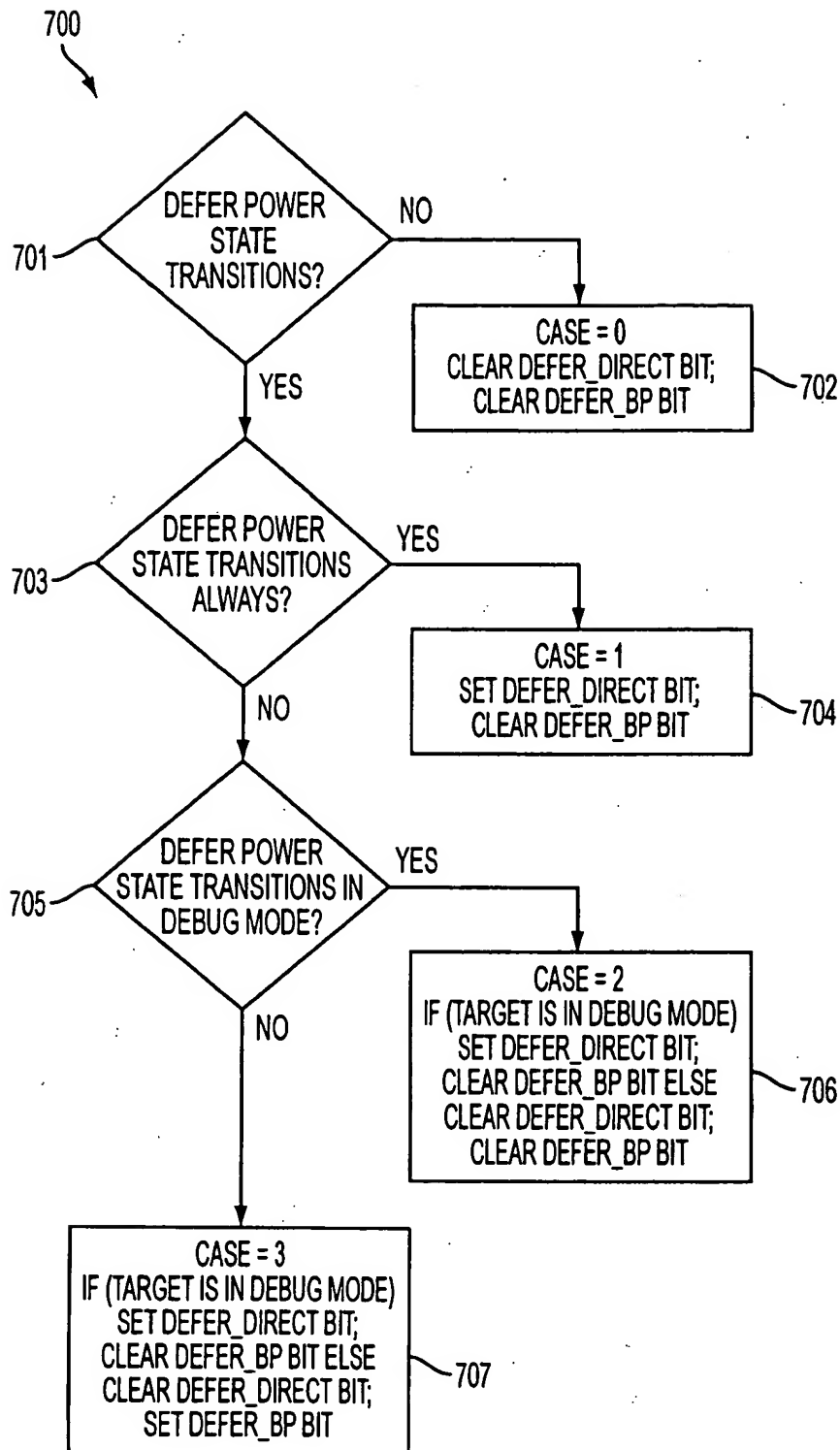


FIG. 7

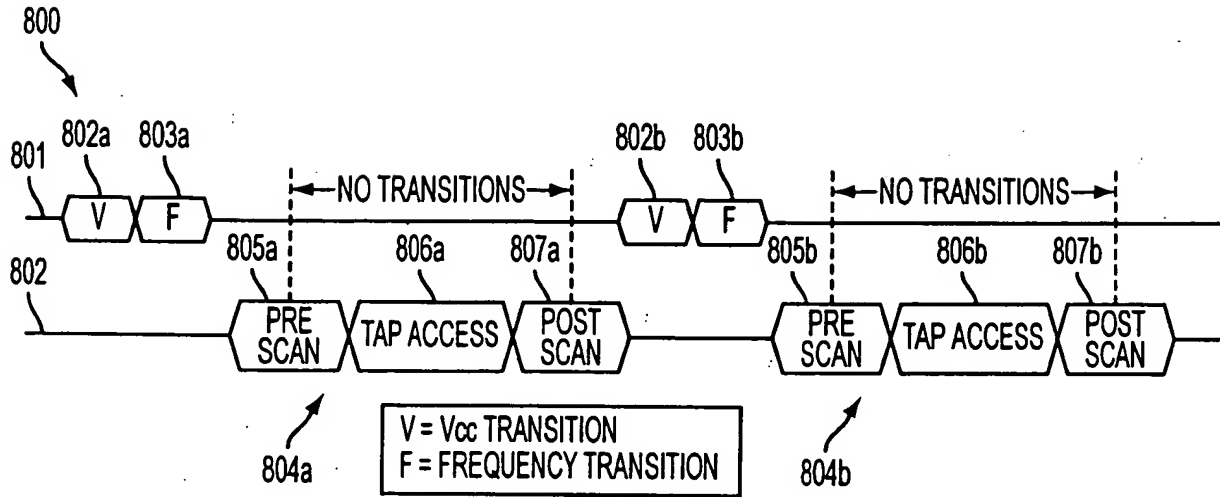


FIG. 8

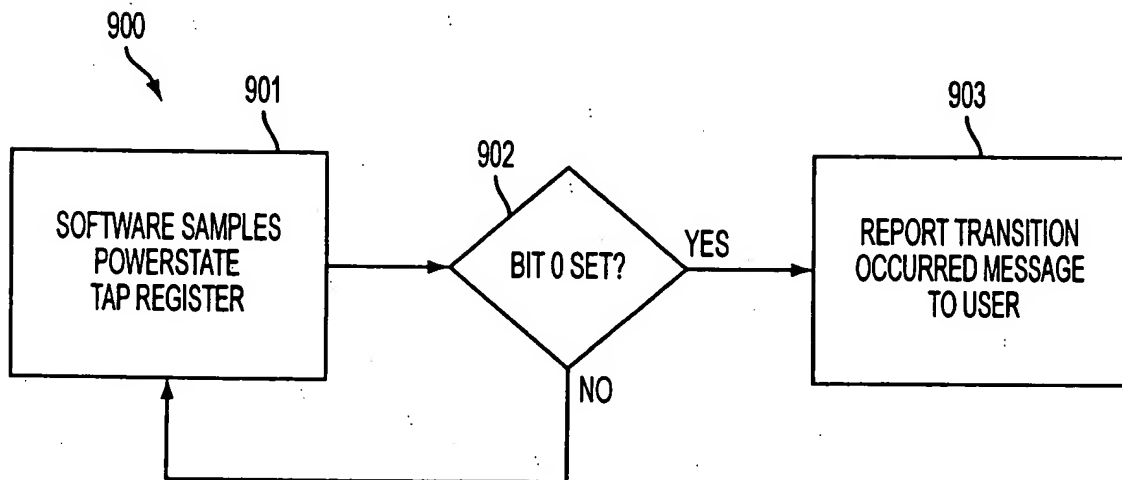


FIG. 9

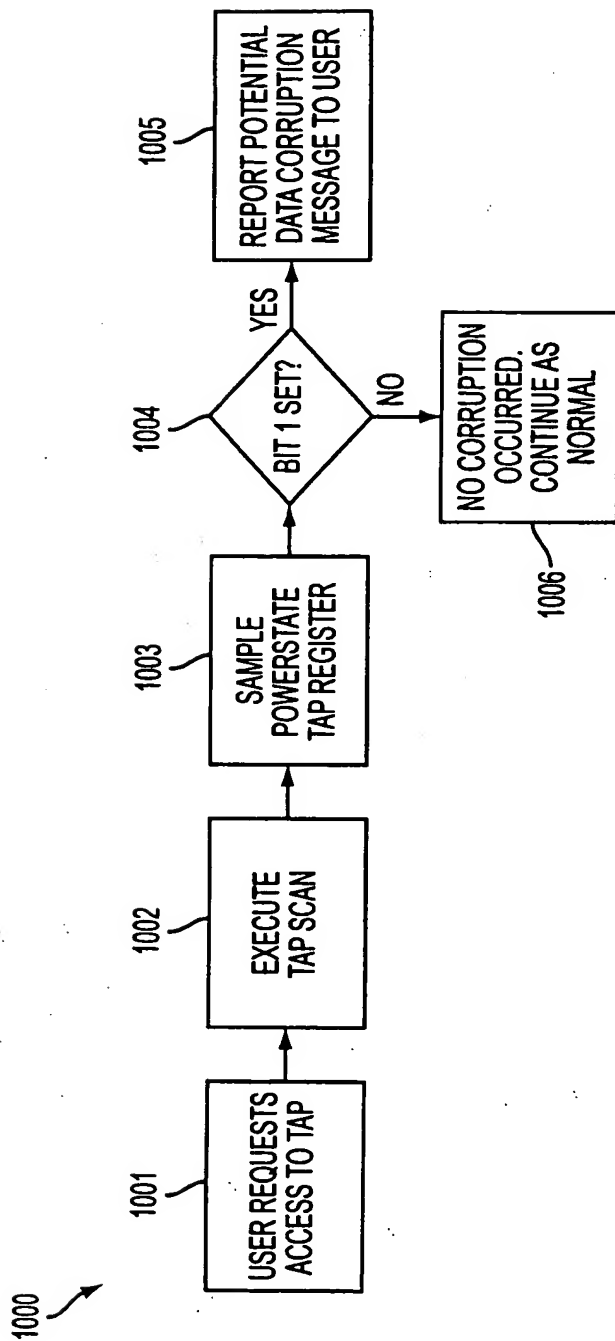


FIG. 10

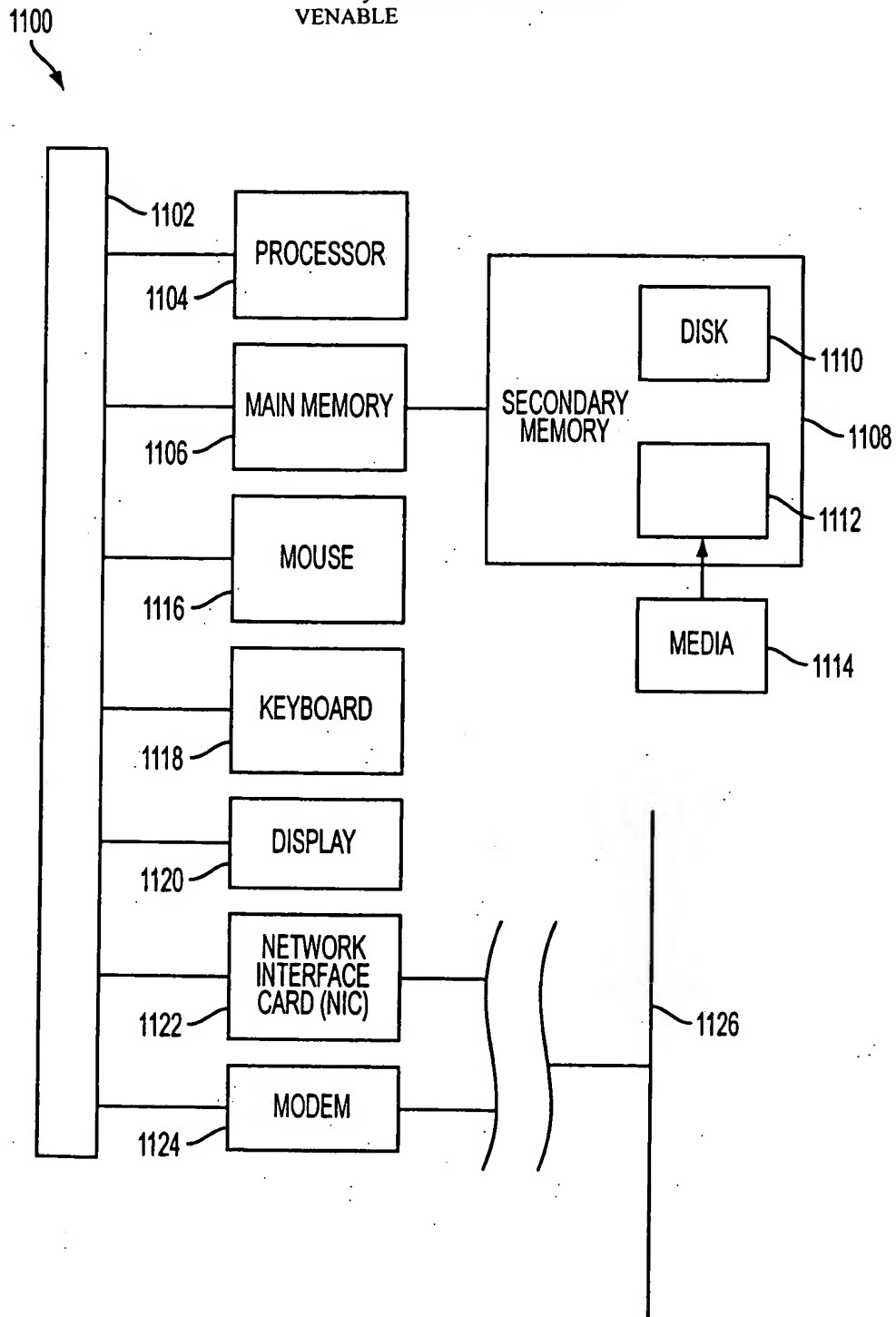


FIG. 11

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VENABLE

PIN NUMBER	HOST PIN NAME	HOST PIN DESCRIPTION	JTAG/TAP? (Y/N)
1	GND	GROUND	N
2	GND	GROUND	N
3	GEN I/O	DATA TRANSMISSION	N
4	DEBUG	DEBUG	N
5	GEN I/O	DATA TRANSMISSION	N
6	DEBUG	DEBUG	N
7	GEN I/O	DATA TRANSMISSION	N
8	GND	GROUND	N
9	GEN I/O	DATA TRANSMISSION	N
10	TDI	TEST DATA IN	Y
11	GEN I/O	DATA TRANSMISSION	N
12	TMS	TEST MODE SELECT	Y
13	GEN I/O	DATA TRANSMISSION	N
14	TRST _n	TEST LOGIC RESET	Y
15	RESET _n	RESET	N
16	TCK	TEST CLOCK	Y
17	DEBUG	DEBUG	N
18	DEBUG	DEBUG	N
19	BCLK _p	BUS CLOCK	N
20	GND	GROUND	N
21	BCLK _n	BUS CLOCK	N
22	PWR	POWER	N
23	GEN I/O	DRIVES GEN I/O	N
24	TDO	TEST DATA OUT	Y
25	GND	GROUND	N
26	PULLED PIN	PULLED PIN	N

FIG. 12

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Title of Invention: Debugging Power
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VENABLE

PIN NUMBER	HOST PIN NAME	TARGET PIN NAME	TARGET PIN DESCRIPTION
1	GND	GND	GROUND
2	GND	GND	GROUND
3	GEN I/O	SLP#	SLEEP STATE
4	DEBUG	SYSTEM ERROR	SYSTEM ERROR
5	GEN I/O	STPCLK#	STOP CLOCK
6	DEBUG	SYSTEM RESET	SYSTEM RESET
7	GEN I/O	GEN I/O	DATA TRANSMISSION
8	GND	GND	GROUND
9	GEN I/O	GEN I/O	DATA TRANSMISSION
10	TDI	TDI	TEST DATA IN
11	GEN I/O	GEN I/O	DATA TRANSMISSION
12	TMS	TMS	TEST MODE SELECT
13	GEN I/O	GEN I/O	DATA TRANSMISSION
14	TRST _n	TRST#	TEST RESET
15	RESET _n	RESET#	RESET
16	TCK	TCK	TEST CLOCK
17	DEBUG	TCK	TEST CLOCK
18	DEBUG		
19	BCLK _p	BCLK0	BUS CLOCK
20	GND	GND	GROUND
21	BCLK _n	BCLK1	BUS CLOCK
22	PWR	PWR	POWER
23	GEN I/O DR	GEN I/O DR	DRIVES GEN I/O
24	TDO	TDO	TEST DATA OUT
25	GND	GND	GROUND
26	PULLED PIN	PULLED PIN	GROUND

FIG. 13